**ABSTRACT**

A method and system for packet ordering in a multi-processor data processing system. The multi-processor system comprises an input queue, packet memory for storing the data packets, a series of packet processors with on-chip memory, an output queue, and an ordering buffer. The ordering buffer is provided to maintain strict packet order in the multi-processor system, where the packets are buffered in on-chip memory, but are not necessarily processed in order. The ordering buffer holds a pointer and completion flag for each packet being processed or already processed but not released to the output queue. The ordering buffer allows the data packets to be read from the on-chip memory in the packet processors regardless of the order in which the data packets are processed. A processed data packet is released to the output queue in order once the processing of earlier packets is completed.